ADCTRIG PAGE 1

1 ;======================================================================

2 ;

3 ; Author : ADI - Apps

4 ;

5 ; Date : April 2002

6 ;

7 ; File : adctrig.asm

8 ;

9 ; Description : Flash led an initial rate of 100ms

10 ; Pressing INTO triggers single conversion

11 ; The ADC result is written to internal memory

12 ; The delay rate is increased

13 ; The program waits for the next INTO to repeat the

14 ; above sequence

15 ;

16 ;======================================================================

17 ;

18 $MOD814 ; Use ADuC814 predefined Symbols

0004 19 CHAN EQU 04H

20

21

---- 22 CSEG ; Defines the following as a segment of code

0000 23 ORG 0000H ; Load Code at '0'

24

0000 020012 25 JMP MAIN ; Jump to MAIN

26 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

27 ;INT0 ISR

0003 28 ORG 0003h ; (INT0 ISR)

0003 D2DC 29 SETB SCONV ; INITIATE A MAIN ADC SINGLE CONVERSION

0005 30DFFD 30 JNB ADCI,$ ; Wait for conversion results

0008 C2DF 31 CLR ADCI ; Clear ADC interrupt flag

32

000A A6DA 33 MOV @R0,ADCDATAH ; Write ADC Result to memory

000C 08 34 INC R0

000D A6D9 35 MOV @R0,ADCDATAL

000F 08 36 INC R0

37

0010 04 38 INC A ; Increment delay

39

0011 32 40 RETI ; Return from Interrupt

41

42

43

44 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

45 ; DELAY

0012 46 MAIN: ; Configure ADC

0012 75EF80 47 MOV ADCCON1,#080h ; power up ADC

0015 75D804 48 MOV ADCCON2,#CHAN ; select channel to convert

49

0018 75FD0D 50 MOV DACCON,#0DH ; Turn DAC0 on

001B 75FA08 51 MOV DAC0H,#08H ;

001E 75F900 52 MOV DAC0L,#00H ; mid-scale

53

0021 7880 54 MOV R0,#80h ; save data at 80h

55

0023 D288 56 SETB IT0 ; INT0 edge triggered

0025 D2AF 57 SETB EA ; enable inturrupts

0027 D2A8 58 SETB EX0 ; enable INT0

ADCTRIG PAGE 2

59

0029 7401 60 MOV A,#01H ; Initialize A -> 1

002B 61 BLINK:

002B B2B3 62 CPL P3.3 ; blink LED

002D 120032 63 CALL DELAY

0030 012B 64 AJMP BLINK

65

66 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

67 ; DELAY

0032 68 DELAY: ; Delays by 100ms \* A

0032 FB 69 MOV R3,A ; Acc holds delay variable

0033 7922 70 DLY0: MOV R1,#022h ; Set up delay loop0

0035 7AFF 71 DLY1: MOV R2,#0FFh ; Set up delay loop1

0037 DAFE 72 DJNZ R2,$ ; Dec R2 & Jump here until R2 is 0

0039 D9FA 73 DJNZ R1,DLY1 ; Dec R1 & Jump DLY1 until R1 is 0

003B DBF6 74 DJNZ R3,DLY0 ; Dec R0 & Jump DLY0 until R0 is 0

003D 22 75 RET ; Return from subroutine

76 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

77

78 END

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80

81

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

ADCTRIG PAGE 3

ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

ADCDATAH . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCDATAL . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

ADCI . . . . . . . . . . . . . . B ADDR 00DFH PREDEFINED

BLINK. . . . . . . . . . . . . . C ADDR 002BH

CHAN . . . . . . . . . . . . . . NUMB 0004H

DAC0H. . . . . . . . . . . . . . D ADDR 00FAH PREDEFINED

DAC0L. . . . . . . . . . . . . . D ADDR 00F9H PREDEFINED

DACCON . . . . . . . . . . . . . D ADDR 00FDH PREDEFINED

DELAY. . . . . . . . . . . . . . C ADDR 0032H

DLY0 . . . . . . . . . . . . . . C ADDR 0033H

DLY1 . . . . . . . . . . . . . . C ADDR 0035H

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EX0. . . . . . . . . . . . . . . B ADDR 00A8H PREDEFINED

IT0. . . . . . . . . . . . . . . B ADDR 0088H PREDEFINED

MAIN . . . . . . . . . . . . . . C ADDR 0012H

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

SCONV. . . . . . . . . . . . . . B ADDR 00DCH PREDEFINED